Xifan Tang

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Major Achievements

1. Accomplished tape-outs for 8 FPGA chips with silicon proofs
2. Developed methodologies and EDA tools for automated FPGA tape-outs
3. Active contributors to open-source projects:
   - OpenFPGA - Inventor & Maintainer
   - Open-source eFPGA IPs - Inventor & Maintainer
   - Verilog-to-Routing - Contributor

Industry Experience

RapidFlex US **Los Gatos, U.S.A.**
CTO and Cofounder *01/2023–Present*

Rapidsilicon **Los Gatos, U.S.A.**
Chief Engineer and Cofounder *08/2021–12/2022*

ReRouting LLC **Salt Lake City, U.S.A.**
Engineer and Cofounder *06/2019–02/2021*

Melexis Technology SA **Bevaix, Switzerland**
Intern *10/2012–12/2012*
Supervisor: Christophe Guillaume-Gentil.
Project: Modeling a Near-Field Communication (NFC) Chip with Verilog-A HDL.

Research Experience

University of Utah **Salt Lake City, U.S.A.**
Adjunct Professor *01/2022–06/2022*

University of Utah **Salt Lake City, U.S.A.**
Research Assistant Professor *01/2020–07/2021*
Supervisor: Prof. Pierre-Emmanuel Gaillardon.
Lead the technical work in the OpenFPGA project, collaborating with industrial and academic partners, i.e., Google, QuickLogic and University of Toronto

University of Utah **Salt Lake City, U.S.A.**
Post-doctoral Researcher *04/2018–12/2019*
Supervisor: Prof. Pierre-Emmanuel Gaillardon.
Lead the technical work in the OpenFPGA project

École Polytechnique Fédérale de Lausanne (EPFL) **Lausanne, Switzerland**
Doctorate Research Assistant *09/2013–03/2018*

Supervisor: Prof. Giovanni De Micheli and Prof. Pierre-Emmanuel Gaillardon.
Doctoral Thesis: Circuit Design, architecture exploration and EDA for FPGAs
Master Thesis: Reconfigurable Architecture Design Based Ambipolar Logic

École Polytechnique Fédérale de Lausanne (EPFL) **Lausanne, Switzerland**
Graduate Research Assistant *09/2011–06/2013*
Supervisors: Prof. Giovanni De Micheli and Prof. Vasilis F. Pavlidis.

Fudan University **Shanghai, China**
Research Assistant *08/2009–07/2011*
Supervisors: Prof. Lingli Wang
Thesis: The Effect of LUT size on Nanometer FPGA Architecture

Education

École Polytechnique Fédérale de Lausanne (EPFL) **Lausanne, Switzerland**
PhD in Computer Science *09/2013–11/2017*
Thesis Title: Circuit Designs, Architecture and CAD for RRAM-based FPGAs

École Polytechnique Fédérale de Lausanne (EPFL) **Lausanne, Switzerland**
Master in Electrical Engineering, 5.23/6 *09/2011–06/2013*
Thesis Title: Reconfigurable Architecture Design Based Ambipolar Logic

Fudan University **Shanghai, China**
Bachelor in Sicence, 3.38/4 *09/2007–06/2011*
Thesis Title: Power Modeling and Optimization for FPGA Routing Resources

Awards and Honnors

Best Contribution Award, Workshop on Open-Source EDA Technology (WOSET) 2020
Outstanding Research Award by Chinese Association for Science and Technology in Utah 2019
Chinese Government Award for Outstanding Self-Financed Students Abroad 2015
500 awardees worldwide and 14 in Switzerland in 2015
Best paper award nomination at *Intl' Conf. on Field Programmable Technology* (ICFPT) 2014
4 papers were nominated from 76 accepted papers
EPFL EDIC Fellowship 2013
Wangdao Scholar honored by FDUROP 2010-2011
Third Prize of Excellent Students at Fudan University 2010-2011
Third Prize of Excellent Students at Fudan University 2007-2008

Books

[B1] Kaihui Tu, **Xifan Tang**, Cunxi Yu, Lana Josipović, Zhufei Chu, *FPGA EDA: Design Principles and Implementation*, Springer, 2024. ISBN-13: 978-9819977543.
[B2] A. Levisse, **Xifan Tang**, P.-E. Gaillardon, *Innovative Memory Architectures Using Functionality Enhanced Devices*, in *Emerging Computing: From Devices to Systems: Looking Beyond Moore and Von Neumann*, Springer, 2022. ISBN-13: 978-9811674877.
[B3] J. Vieria, E. Giacomin, Y. Qureshi, M. Zapater, **Xifan Tang**, S. Kvatinsky, D. Atienza, P.-E. Gaillardon, *Accelerating Inference on Binary Neural Networks with Digital RRAM Processing*, in *VLSI-SoC: New Technology Enabler*, IFIP Advances in Information and Communication Technology (IFIPAICT), pp. 257-278, 2020.

[B4] **Xifan Tang**, P.-E. Gaillardon, I. O'Connor, G. De Micheli, *Ultrafine grain FPGAs with Polarity controllable Transistors*, in *Functionality-Enhanced Devices: An alternative to Moore's Law* (Ed.: P.-E. Gaillardon), The Institution of Engineering and Technology (IET), pp. 273-298, 2018.
[B5] **Xifan Tang**, P.-E. Gaillardon, I. O'Connor, G. De Micheli, *Ultrafine grain FPGAs with Polarity controllable Transistors*, in *Functionality-Enhanced Devices: An alternative to Moore's Law* (Ed.: P.-E. Gaillardon), The Institution of Engineering and Technology (IET), pp. 273-298, 2018.
[B6] **Xifan Tang**, S. Rahimian Omam, P. Meinerzhagen, P.-E. Gaillardon and G. De Micheli, *Low Power FPGAs based on Resistive Memories*, in P.-E. Gaillardon, Editor, *Reconfigurable Logic: Architecture, Tools and Applications*, CRC press, 28th October 2015, pp. 399-432.

Journal Publications (fully refereed)

[J1] J. Bhandari, AKT Moosa, B. Tan, C. Pilato, G. Gore, **Xifan Tang**, S. Temple, P.-E. Gaillardon, R. Karri, *Not all fabrics are created equal: Exploring eFPGA parameters for IP redaction*, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 31, no. 10, pp. 1459-1471, October 2023.
[J2] G. Gore, **Xifan Tang**, P.-E. Gaillardon, *A Scalable and Area-Efficient Configuration Circuitry for Semi-Custom FPGA Design*, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 31, no. 8, pp. 1128-1139, August 2023.
[J3] **Xifan Tang**, E. Giacomin, A. Alacchi, B. Chauviere, P.-E. Gaillardon, *OpenFPGA: An Open-source Framework for Agile Prototyping Customizable FPGAs*, IEEE Micro, vol. 40, no. 4, pp. 41-48, 1 July-Aug. 2020. (In the list of top 50 most popular papers in September 2020 - January 2021, and top 10 most popular papers in July-August 2020)
[J4] **Xifan Tang**, E. Giacomin, G. De Micheli and P.-E. Gaillardon, *FPGA-SPICE: A Simulation-based Architecture Evaluation Framework for FPGAs*, IEEE Transactions on VLSI (Very Large Scale Integration) Systems (TVLSI), Vol. 27, No. 3, pp. 637-650, Mar. 2019. (In the list of top 10 most popular papers from February 2019 to April 2020)
[J5] **Xifan Tang**, E. Giacomin, G. De Micheli and P.-E. Gaillardon, *Post-P&R Performance and Power Analysis for RRAM-based FPGAs*, IEEE Journal on Emerging and Selected Topics in Circuits and Systems, Vol. 8, No. 3, pp. 639-650, Sept. 2018.
[J6] **Xifan Tang**, E. Giacomin, G. De Micheli and P.-E. Gaillardon, *Circuit Designs of High-performance and Low-power RRAM-based Multiplexers based on 4T(ransistor)1R(RAM) Programming Structure*, IEEE Transaction on Circuits and Systems I: Regular Papers (TCAS-I), Vol. 64, No. 5, 2017, pp. 1173-1186. (In the list of top 50 most popular papers in May 2017)
[J7] **Xifan Tang**, P.-E. Gaillardon and G. De Micheli, *A High-performance FPGA Architecture Using One-level RRAM-based Multiplexers*, IEEE Transaction on Emerging Topics in Computing (TETC), Vol. 5, No. 2, pp. 210-222. (In the list of top 50 most popular papers from June to November 2017)
[J8] **Xifan Tang**, K. Gain, P.-E. Gaillardon and G. De Micheli, *A Study on the Programming Structures for RRAM-based FPGA Architectures*, IEEE Transaction on Circuits and Systems I: Regular Papers (TCAS-I), Vol. 63, No. 4, 2016, pp. 503-516. (In the list of top 50 most popular papers in April 2016, and top 10 most popular papers in May 2016)
[J9] P.-E. Gaillardon, **Xifan Tang**, G. Kim and G. De Micheli, *A Novel FPGA Architecture Based on Ultrafine Grain Reconfigurable Logic Cells*, IEEE Transactions on VLSI (Very Large Scale Integration) Systems (TVLSI), Vol. 23, No. 10, 2015, pp. 1063-8210.

[J10] J. Zhang, **Xifan Tang**, P.-E. Gaillardon and G. De Micheli, *Configurable Circuits Featuring Dual-Threshold-Voltage Design With Three-Independent-Gate Silicon Nanowire FETs*, IEEE Transaction on Circuit And Systems Part 1: Regular Papers (TCAS-I), Vol. 61, No. 10, 2014, pp. 2851-2861.
[J11] Hu Xu, V. F. Pavlidis, **Xifan Tang**, Wayne P. Burleson, G. De Micheli, *Timing Uncertainty in 3-D Clock Trees due to Process Variations and Power Supply Noise*, IEEE Transactions on VLSI (Very Large Scale Integration) Systems (TVLSI), Vol. 21, No. 12, pp. 2226-2239, 2013.
[J12] S. Rahimian Omam, V. F.Pavlidis, **Xifan Tang** and G. De Micheli, *An Enhanced Design Methodology for Resonant Clock Trees*, Journal of Low Power Electronics, Vol. 9, No. 2, pp. 198-206, 2013.

Conference Publications (fully refereed)

[C1] A. Mishra, N. Rao, G. Gore and **Xifan Tang**, *Architecture Exploration of Heterogeneous FPGAs for Performance Enhancement of ML Benchmarks*, IEEE Asia Pacific Conference on Circuits and Systems, 2023, pp. 232-235.
[C2] C. Tomajoli,L. Collini, J. Bhandari, A. Moosa, B. Tan, **Xifan Tang**, P.-E. Gaillardon, R. Karri, C. Pilato, *ALICE: An automatic design flow for eFPGA redaction*, ACM/IEEE Design Automation Conference (DAC), 2022, pp. 781-786.
[C3] S. Temple, W. L. Neto, A. Snelgrove, **Xifan Tang**, P.-E. Gaillardon, *Getting the Most out of your Circuits with Heterogeneous Logic Synthesis*, ACM/IEEE Design Automation Conference (DAC), Virtual, 2021, pp. 1331-1334.
[C4] J. Bhandari, A. Khader, B. Tan, C. Pilato, G. Gore, **X. Tang**, S. Temple, P.-E. Gaillardon and R. Karri, *Exploring eFPGA-based Redaction for IP Protection*, International Conference On Computer Aided Design, Virtual, 2021, in press.
[C5] **X. Tang**, G. Gore, G. Brown, P.-E. Gaillardon, *Taping out an FPGA in 24 hours with OpenFPGA: The SOFA Project*, IEEE International Conference on Field Programmable Logic and Applications (FPL), Dresden, Germany, 2021, in press.
[C6] A. Alacchi, E. Giacomin, **X. Tang**, P.-E. Gaillardon, *Smart-Redundancy: an Alternative SEU/Set Mitigation Method for FPGAs*, IEEE International Symposium on Circuits and Systems (ISCAS), 23-26 May 2021, Daegu, Korea..
[C7] G. Gore, **X. Tang**, P.-E. Gaillardon, *A Scalable and Robust Hierarchical Floorplanning to Enable 24-hour Prototyping for 100k-LUT FPGAs*, International Symposium on Physical Design (ISPD), 21-24 March 2021, Virtual.
[C8] M. Austin, S. Temple, W. Lau, L. Amaru, **Xifan Tang** and P.-E. Gaillardon, *A Scalable Mixed Synthesis Framework for Heterogeneous Networks*, Design, Automation and Test in Europe Conference and Exhibition (DATE), Grenoble, France, 2020.
[C9] **Xifan Tang**, E. Giacomin, A. Alacchi and P.-E. Gaillardon, *A Study on Switch Block Patterns for Tileable FPGA Routing Architectures*, IEEE International Conference on Field Programmable Technology (FPT), Tianjin, China, 2019, pp. 247-250.
[C10] **Xifan Tang**, E. Giacomin, A. Alacchi, B. Chauviere and P.-E. Gaillardon, *OpenFPGA: An Opensource Framework Enabling Rapid Prototyping of Customizable FPGAs*, IEEE International Conference on Field Programmable Logic and Applications (FPL), Barcelona, Spain, 2019, pp. 367-374. (acceptance rate: 18.5%)
[C11] Walter L. N.,**Xifan Tang**, M. Austin, L. Amaru and P.-E. Gaillardon, *Improving Logic*

Optimization in Sequential circuits using Majority-inverter Graphs, IEEE Computer Society Annual Symposium on VLSI (ISVLSI), 15-17 July 2019, Miami, FL, USA..
[C12] J. Vieira, E. Giacomin, Y. Mahmood Qureshi, M. Zapater, **Xifan Tang**, S. Kvatinsky, D. Atienza and P.-E. Gaillardon, *A Product Engine for Energy-Efficient Execution of Binary Neural Networks Using Resistive Memories*, 27th IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC), 6-9 October 2018, Cusco, Peru..
[C13] **Xifan Tang**, G. De Micheli and P.-E. Gaillardon, *Optimization Opportunities in RRAM-based FPGA Architectures*, IEEE Latin American Symposium on Circuits and Systems (LASCAS), 2017, pp. 281-284.
[C14] **Xifan Tang**, E. Giacomin, G. De Micheli and P.-E. Gaillardon, *Physical Design Considerations of One-level RRAM-based Routing Multiplexers*, ACM/SIGDA International Symposium on Physical Design (ISPD), 2017, pp. 47-54.
[C15] Z. Chu, **Xifan Tang**, M. Soeken, A. Petkovska, G. Zgheib, L. Amarú, Y. Xia, P. Ienne, G. De Micheli, and P.-E. Gaillardon, *Improving Circuit Mapping Performance Through MIG-based Synthesis for Carry Chains*, ACM Great Lakes Symposium on VLSI 2017 (GLSVLSI), New York, NY, USA, 131-136.
[C16] **Xifan Tang**, P.-E. Gaillardon and G. De Micheli, *A Full-capacity Local Routing Architecture for FPGAs*, ACM/SIGDA International Symposium on Field Programmable Gate Arrays (FPGA), Monterey, U.S.A, 2016, pp. 281-281.
[C17] **Xifan Tang**, P.-E. Gaillardon and G. De Micheli, *FPGA-SPICE: A Simulation-based Power Estimation Framework for FPGAs*, ACM/SIGDA International Conference on Computer Design (ICCD), New York, U.S.A., 2015, pp. 696-703.
[C18] **Xifan Tang**, P.-E. Gaillardon and G. De Micheli, *Accurate Power Analysis for Near-Vt RRAM-based FPGA*, IEEE Field Programmable Logic and Applications (FPL), London, United Kingdom, 2015, pp. 1-4.
[C19] P.-E. Gaillardon, **Xifan Tang**, J. Sandrini, M. Thammasack, S. Rahimian Omam, D. Sacchetto, Y. Leblebici and G. De Micheli, *A Ultra-low-power FPGA based on Monolithically Integrated RRAMs*, Design, Automation and Test in Europe Conference and Exhibition (DATE), Grenoble, France, 2015, pp. 1203-1208. (Invited Paper)
[C20] P.-E. Gaillardon, G. Kim, **Xifan Tang**, L. Amaru and G. De Micheli, *Towards More Efficent Logic Blocks By Exploiting Biconditional Expansion*, ACM/SIGDA International Symposium on Field Programmable Gate Arrays (FPGA), Monterey, U.S.A, 2015, pp. 262-262.
[C21] S. Rahimian Omam, **Xifan Tang**, P.-E. Gaillardon and G. De Micheli, *A Study on Buffer Distribution for RRAM-based FPGA Routing Structures*, IEEE Latin American Symposium on Circuit And Systems (LASCAS), Montevideo, Uruguay, 2015, pp. 1-4.
[C22] **Xifan Tang**, P.-E. Gaillardon and G. De Micheli, *A High-performance Low-power Near-Vt RRAM-based FPGA*, IEEE Field Programmable Technology (FPT), Shanghai, China, 2014, pp. 207-214. (Best paper nomination)
[C23] **Xifan Tang**, P.-E. Gaillardon and G. De Micheli, *Pattern-base Logic Block and Clustering Algorithm*, IEEE Field Programmable Logic and Applications (FPL), Munich, Germany, 2014, pp.1-4.
[C24] **Xifan Tang**, J. Zhang, P.-E. Gaillardon and G. De Micheli, *TSPC Flip-flop Circuit Design with Three-Independent-Gate Silicon Nanowire FETs*, International Symposium on Circuit And Systems (ISCAS), Melbourne, Australia, 2014, pp. 1660-1663.
[C25] P.-E. Gaillardon, **Xifan Tang** and G. De Micheli, *Novel Configurable Logic Block Architecture Exploiting Controllable-Polarity Transistors*, IEEE International Symposium on Reconfigurable

and Communication-Centric Systems-on-Chip (ReCoSoC), Montpellier, France, 2014, pp. 1-3. (Invited Paper)
[C26] **Xifan Tang**, L. Wang, *The Effect of LUT Size on Nanometer FPGA Architecture*, IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT), Xi'An, China, 2012, pp. 1-3.
[C27] **Xifan Tang**, L. Wang and H. Xu, *An Accurate Dynamic Power Model on FPGA Routing Resources*, IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT), Xi'An, China, 2012, pp. 1-4.

Workshop and Conference Presentations

[1] **Xifan Tang**, G. Gore, E. Giacomin, A. Alacchi, B. Chauviere and P.-E. Gaillardon, *OpenFPGA: Towards Automated Prototyping for Versatile FPGAs*, International Workshop on Open-Source EDA Technology (WOSET), 5 November 2020, virtual. Best Contribution Award
[2] S. Temple, W. Neto, M. Austin, **Xifan Tang** and P.-E. Gaillardon, *LSOrcale: Using Mixed Logic Synthesis in an Open Source ASIC Design Flow*, International Workshop on Open-Source EDA Technology (WOSET), 5 November 2020, virtual.
[3] M. Austin, W. Lau Neto, L. Amaru, **Xifan Tang** and P.-E. Gaillardon, *Towards a Novel Logic Synthesis Framework Supervised by Convolutional Neural Network*, International Workshop on Logic Synthesis 2019, 21-23 June 2019, Lausanne, Switzerland.
[4] W. Lau Neto, M. Austin, L. Amaru, **Xifan Tang** and P.-E. Gaillardon, *Improving Logic Optimization in Sequential circuits using Majority-inverter Graphs*, International Workshop on Logic Synthesis 2019, 21-23 June 2019, Lausanne, Switzerland.
[5] **Xifan Tang**, *FPGA-SPICE: A Simulation-based FPGA Architecture Exploration Tool Suite*, Ningbo University ECE Seminar, Ningbo, China, March, 2019.
[6] **Xifan Tang**, E. Giacomin, P.-E. Gaillardon and N. Chetrit, *Ultra-low-power RRAM-based FPGA: A Road towards Reconfigurable Edge Computing*, Government Microcircuit Applications & Critical Technology Conference, 25-28 March 2019, Albuquerque, NM, USA..
[7] B. Chauviere, A. Allachi, E. Giacomin, **Xifan Tang**, P.-E. Gaillardon, *OpenFPGA: a Complete Open Source Framework for FPGA Prototyping*, Workshop on Open Source Design Automation (OSDA), 29 March 2019, Florence, Italy..
[8] **Xifan Tang**, P.-E. Gaillardon and N. Chetrit, *High-performance Energy-Efficent FPGA based on Resitive Memories*, U.S. Airforce Science and Technology 2030 Conference, 11 July 2018, University of Utah, Salt Lake City, USA..
[9] **Xifan Tang**, *FPGA-SPICE: A Simulation-based FPGA Architecture Exploration Tool Suite*, Xilinx Seminar, San Jose, March, 2017.
[10] **Xifan Tang**, P.-E. Gaillardon and G. De Micheli, *High Performance Near-Vt RRAM-based FPGA: Opportunities for Low-Power Versatile Computing*, HiPEAC (European Network on High Performance and Embedded Architecture and Compilation), Athens, Greece, October, 2014.

Patents

[P1] **Xifan Tang**, P.-E. Gaillardon and G. De Micheli, *Pattern-based FPGA Logic Block and Clustering Algorithm*, Patent No. US 9971862 (B2), 26 August 2014. Granted.
[P2] P.-E. Gaillardon, **Xifan Tang** and G. De Micheli, *A High-Performance Low-Power Near-Vt*

RRAM-based FPGA, Patent No. US9276573 (B2), 28 July 2014. Granted.
[P3] P.-E. Gaillardon, **Xifan Tang**, Gain Kim, G. De Micheli and Edouard Giacomin, *Resistive Random Access Memory based Multiplexers and Field Programmable Gate Arrays*, Patent No. US10348306 (B2), July 2019. Granted.
[P4] G. Gore, **Xifan Tang**, and P.-E. Gaillardon, *Hierarchical Floor-planning for Rapid FPGA Prototyping*, Patent No. US17/695,093 (A1), March 2022. In press

Professional Service

[1] *Board Member* for the *Open-Source FPGA* (OSFPGA) Foundation
[2] *Programme Committee Member* for the 2020 IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC)
[3] *Programme Committee Member* for the 2019 Euromicro Conference on Digital System Design (DSD)
[4] *Reviewer* for the Elsevier Global Book Production
[5] *Reviewer* for the Bentham eBook Publisher
[6] *Reviewer* for the IEEE Micro
[7] *Reviewer* for IEEE Computer Architecture Letters
[8] *Reviewer* for the IEEE Transactions on Circuits and Systems I: Regular Papers (TCAS-I)
[9] *Reviewer* for the IEEE Transactions on Circuits and Systems II: Express Brief (TCAS-II)
[10] *Reviewer* for the IEEE Transactions on Very Large Scale Integration Systems (TVLSI)
[11] *Reviewer* for the IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)
[12] *Reviewer* for the ACM Computing Surveys (CSUR)
[13] *Reviewer* for the IEEE Transactions on Nanotechnology (TNANO)
[14] *Reviewer* for the IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS)
[15] *Reviewer* for the IEEE Transactions on Knowledge and Data Engineering (TKDE)
[16] *Reviewer* for the IEEE Internet of Things Journal
[17] *Reviewer* for the ACM Journal on Emerging Technologies in Computing Systems (JETCS)
[18] *Reviewer* for the ACM Journal Transactions on Design Automation of Electronic Systems (TODAES)
[19] *Reviewer* for the IET Computers & Digital Techniques
[20] *Reviewer* for the Elsevier Microelectronics Journal
[21] *Reviewer* for the IEEE Access
[22] *Reviewer* for the IEEE Open Journal of the Computer Society
[23] *Reviewer* for the Journal of Signal Processing
[24] *Reviewer* for the Journal of Circuits, Systems and Computers (JCSC)
[25] *Reviewer* for the International Journal of Sensors, Wireless Communications and Control
[26] *Reviewer* for the 2024 IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT)
[27] *Reviewer* for the 2019 IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)
[28] *Reviewer* for the 2018 IEEE Computer Society Annual Symposium on VLSI (ISVLSI)
[29] *Reviewer* for the 2017 IEEE International Symposium on Circuits And Systems (ISCAS)

[30] *Reviewer* for the 2017 IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)

Thesis Advisor

Anubhav Mishra **India**
I.I.I.T. Bangalore *06/2022*
Co-supervisor with Prof. Nanditha Rao
Master Thesis: Architecture Exploration of Heterogeneous FPGAs for Performance Enhancement of ML Benchmarks

Teaching Activity

• FPGA Computer Aided Design 05/2022
PhD course at Fudan University
Guest Lecturer
• Principles of FPGA Architecture and Applications 05/2022
Undergraduate course at Fudan University
Guest Lecturer
• Design Technology for Integrated System 09/2016-12/2016
Master/PhD course at EPFL
Responsible for exercise/homework, laboratory sessions and projects.
• Design Technology for Integrated System 09/2015-12/2015
Master/PhD course at EPFL
Responsible for exercise/homework, laboratory sessions and projects.
• Design Technology for Integrated System 09/2014-12/2014
Master/PhD course at EPFL
Responsible for exercise/homework, laboratory sessions and projects.
• EDA TP 09/2013-12/2013
Master course at EPFL
Responsible for laboratory sessions.

Languages

Chinese: Mother tongue
English: Working Proficiency